What is claimed is:

1. A self-aligned inner gate recess channel in a semiconductor substrate, comprising:

a. a recess trench formed in an active region of the substrate;

b. a gate dielectric layer formed on a bottom portion of the recess trench;

c. recess inner sidewall spacers formed on sidewalls of the recess trench;

d. a gate formed in the recess trench so that an upper portion of the gate protrudes above an upper surface of the substrate, wherein a thickness of the recess inner sidewall spacers causes a center portion of the gate to have a smaller width than the protruding upper portion and a lower portion of the gate;

e. a gate mask formed on the gate layer;

f. gate sidewall spacers formed on the protruding upper portion of gate and the gate mask; and

g. a source/drain region formed in the active region of the substrate adjacent the gate sidewall spacers.

2. The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess trench has a width at an opening thereof of about 900 Å.

3. The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess trench has a depth of between about 1300 - 1800 Å.

4. The self-aligned inner gate recess channel as claimed in claim 1, wherein the substrate comprises:

a shallow trench isolation region; and

the active region includes a well region, a threshold voltage control region, and a source/drain region.

5. The self-aligned inner gate recess channel as claimed in claim 4, wherein the shallow trench isolation region has a depth of approximately 3000 Å.

6. The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate dielectric layer is selected from the group consisting of an oxide layer, an oxynitride layer, an alumina (Al_2O_3) layer, and a ruthenium oxide (RuO) layer.

7. The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate dielectric has a thickness of about 50 Å.

8. The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess inner sidewall spacers have a thickness of about 200 Å.

9. The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess inner sidewall spacers are formed of either silicon oxide or silicon nitride.

10. The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate formed in the recess trench comprises:

a first gate layer formed in a bottom portion of the recess trench; and

a second gate layer formed on the first gate layer in an upper portion of the recess trench, the second gate layer having a lower portion within the recess trench and an upper portion that protrudes above the upper surface of the substrate,

wherein a thickness of the recess inner sidewall spacers causes the lower portion of the second gate layer to have a smaller width than the protruding upper portion of the second gate layer and the first gate layer.

11. The self-aligned inner gate recess channel as claimed in claim 10, wherein the first gate layer is a poly gate layer.

12. The self-aligned inner gate recess channel as claimed in claim 10, wherein the first gate layer has a thickness of about 800 Å.

13. The self-aligned inner gate recess channel as claimed in claim 10, wherein the second gate layer is a poly gate layer.

14. The self-aligned inner gate recess channel as claimed in claim 1, wherein the source/drain region in the active region of the substrate is an n^+ source/drain region.

15. A method of forming a self-aligned inner gate recess channel in a semiconductor substrate, comprising:

a. sequentially depositing an oxide mask layer, a poly mask layer, and a photoresist layer on the substrate having an active region;

b. etching the poly mask layer, the oxide mask layer and the active region of the substrate to form a recess trench;

c. forming recess inner sidewall spacers on sidewalls of the recess trench;

d. etching a bottom portion of the recess trench to increase a depth of the recess trench;

e. enlarging a width of the bottom portion of the recess trench below the recess inner sidewall spacers;

f. forming a gate dielectric on the bottom portion of the recess trench;

g. forming a gate in the recess trench so that an upper portion of the gate protrudes above an upper surface of the substrate, wherein a

thickness of the recess inner sidewall spacers causes a center portion of the gate to have a smaller width than the protruding upper portion and a lower portion of the gate;

h. forming a gate mask on the gate;

i. forming gate sidewall spacers on the protruding upper portion of the gate and the gate mask; and

j. performing an ion implantation process to form a source/drain region in the active region of the substrate adjacent the gate sidewall spacers.

16. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, further comprising:

enlarging a lower portion of the recess trench, prior to forming the recess inner sidewall spacers on sidewalls of the recess trench.

17. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the source/drain region in the active region of the substrate is an n^+ source/drain region.

18. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the oxide mask layer has a thickness of about 200 Å.

19. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the poly mask is a poly hard mask.

20. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the poly mask layer is formed by a low pressure chemical vapor deposition (LPCVD) process.

21. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the poly mask layer has a thickness of about 1000 Å.

22. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the substrate comprises:

a shallow trench isolation region; and

the active region includes a well region, a threshold voltage control region, and a source/drain region.

23. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 22, wherein the shallow trench isolation region is formed to a depth of about 3000 Å.

24. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 22, wherein the recess trench has a width at an opening thereof of about 900 Å.

25. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein etching the poly mask layer, the oxide mask layer and the active region of the substrate to form the recess trench comprises:

etching the poly mask layer using the photoresist layer as a mask and removing the photoresist layer; and

etching the active region of the substrate using the etched poly mask layer as a mask to form the recess trench and removing the poly mask layer.

26. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein enlarging the lower width of the recess trench is performed using a chemical dry etching (CDE) process.

27. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the bottom portion of the recess trench is enlarged to a width of about 900 Å.

28. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the recess inner sidewall spacers have a thickness of about 200 Å.

29. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein forming the recess inner sidewall spacers comprises:

depositing a spacer layer on the substrate and the recess trench using a LPCVD process; and

anisotropically etching the spacer layer to form the recess inner sidewall spacers on the sidewalls of the recess trench.

30. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the etching to increase the depth of the recess trench is an anisotropic etching process.

31. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the depth of the recess trench is increased by about 300 Å.

32. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the total depth of the recess trench after increasing the depth of the recess trench is between about 1300 - 1800 Å.

33. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the width of the bottom portion of the recess trench is enlarged using a chemical dry etching (CDE) process.

34. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the width of the bottom portion of the recess trench is enlarged to a width of about 900 Å.

35. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the gate dielectric is selected from the group consisting of an oxide layer, an oxynitride layer, an alumina (Al_2O_3) layer, and a ruthenium oxide (RuO) layer.

36. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the gate dielectric is formed using a thermal oxidation process.

37. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the gate dielectric has a thickness of about 50 Å.

38. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 15, wherein the gate is formed by depositing a gate layer using a LPCVD process and etching the gate layer.

39. A method of forming a self-aligned inner gate recess channel in a semiconductor substrate, comprising:

a. sequentially depositing an oxide mask layer, a poly mask layer, and a photoresist layer on the substrate having an active region;

b. etching the poly mask layer, the oxide mask layer and the active region of the substrate to form a recess trench;

c. forming a gate dielectric layer within the recess trench;

d. forming and etching a first gate layer to partially fill a lower portion of the recess trench;

e. forming recess inner sidewall spacers on sidewalls of an upper portion of the recess trench above the first gate layer;

f. forming and etching a second gate layer on the first gate layer to form a gate in the recess trench so that an upper portion of the second gate layer protrudes above an upper surface of the substrate, wherein a thickness of the recess inner sidewall spacers causes a lower portion of the second gate layer to have a smaller width than the protruding upper portion of the second gate layer and the first gate layer;

g. forming a gate mask on the second gate layer;

h. forming gate sidewall spacers on the protruding upper portion of the second gate layer and the gate mask; and

i. performing an ion implantation process to form a source/drain region in the active region of the substrate adjacent the gate sidewall spacers.

40. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, further comprising:

enlarging a bottom portion of the recess trench, prior to forming the gate dielectric layer within the recess trench.

41. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the source/drain region in the active region of the substrate is an n^+ source/drain region.

42. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the oxide mask layer has a thickness of about 200 Å.

43. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the poly mask is a poly hard mask.

44. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the poly mask layer is formed by a low pressure chemical vapor deposition (LPCVD) process.

45. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the poly mask layer has a thickness of about 1000 Å.

46. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the substrate comprises:

a shallow trench isolation region; and

the active region includes a well region, a threshold voltage control region, and a source/drain region.

47. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 46, wherein the shallow trench isolation region is formed to a depth of about 3000 Å.

48. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the etching to form the recess trench is an isotropic etching process.

49. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the recess trench has a depth of about 1500 Å.

50. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 40, wherein the enlarging the lower width portion of the recess trench is performed using a chemical dry etching (CDE) process.

51. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 40, wherein the lower width of the recess trench is enlarged to a width of about 900 Å.

52. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the gate dielectric layer is selected from the group consisting of an oxide layer, an oxynitride layer, an alumina (Al_2O_3) layer, and a ruthenium oxide (RuO) layer.

53. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the gate dielectric layer is formed by a thermal oxidation process.

54. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the gate dielectric layer has a thickness of about 50 Å.

55. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the first gate layer is a poly gate layer.

56. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the first gate layer has a thickness of about 800 Å.

57. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein forming the first gate layer comprises:

depositing a first gate layer on the substrate and recess trench to fill the recess trench; and

performing an etchback process on the first gate layer until the first gate layer remains only in the lower portion of the recess trench.

58. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 57, wherein the first gate layer is deposited using a LPCVD process.

59. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the recess inner sidewall spacers have a thickness of about 200 Å.

60. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein forming the recess inner sidewall spacers comprises:

depositing a spacer layer on the substrate and the recess trench using a LPCVD process; and

anisotropically etching the spacer layer to form the recess inner sidewall spacers on the sidewalls of the recess trench.

61. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 60, wherein the spacer layer is either a silicon oxide layer or a silicon nitride layer.

62. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the second gate layer is a poly gate layer.

63. The method of forming a self-aligned inner gate recess channel in a semiconductor substrate as claimed in claim 39, wherein the second gate layer is formed by a LPCVD process.